

REMARKS

Claims 1-8 are pending in this application. Claims 1, 3, 4, and 5 are amended herein. Claims 6, 7, and 8 are added herein. Support for the amendments to the claims, and for the new claims, may be found in the claims as originally filed and at page 24, lines 12-21 of the specification. Reconsideration is requested based on the foregoing amendment and the following remarks.

Response to Arguments:

The Applicants appreciate the consideration given to their arguments. The Applicants, however, are disappointed that their arguments were not found to be persuasive. The final Office Action asserts that the standard register of Gottlieb is shared in the sense that, when a thread is active, it uses the standard register file, and when it is replaced in the standard register file by another active thread, it becomes inactive and resides in the shadow register. The perception of the claimed invention illustrated by the final Office Action, and particularly the recitation "in common", appears to be that several programs using hardware in *serial* order amounts to use of that hardware *in common*. This is submitted to be incorrect.

"In common," rather, implies substantially simultaneous or parallel use. Gottlieb, in fact, rules out the use of hardware in common by a plurality of programs when he defines coarse grained multithreading as "having the processor support only one active thread at a time by limiting instructions from only one thread in the execution pipeline," at column 1, lines 43-46, and then limits his invention to coarse grained multithreaded applications only at column 2, lines 39-43. Further reconsideration is thus requested.

Claim Rejections - 35 U.S.C. § 102:

Claims 1-5 were rejected under 35 U.S.C. § 102(e) as anticipated by US Patent No. 6,298,431 to Gottlieb (hereinafter "Gottlieb"). The rejection is traversed to the extent it would apply to the claims as amended.

Claim 1 recites,

"the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer."

Gottlieb neither teaches, discloses, nor suggests "the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer," as recited in claim 1. As shown in Fig. 3 of Gottlieb, rather, the standard register

cell 20 is coupled to the banked shadowed registers 34-38. This implies that the contents of the standard register cell 20 can only be evacuated to the banked shadowed registers 34-38. This also implies that the contents of the standard register cell 20 can only be restored from the banked shadowed registers 34-38. In particular, as described at column 6, lines 10-16,

Referring now to FIG. 3, shown is a circuit diagram illustrating one implementation of the banked shadowed register file 30 shown in FIG. 2. In this embodiment, each register comprises a pair of inverters disposed in parallel and juxtaposed relation. This includes the standard register cell 20, the temporary registers 44, 46, and the banked shadowed registers 34-38.

Thus Gottlieb can only switch between four separate threads. This is to be contrasted with claim 1, which recites, "the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer."

Furthermore, in Gottlieb, the banked shadowed register file 30 comprises a first register 34, a second register 36, and a third register 38. In particular, as described at column 4, lines 42-47,

For each register cell 20 in the standard register file 18, the banked shadowed register file 30 comprises a first register 34, a second register 36, a third register 38, first and second transmission gates 40, 42, and first and second temporary registers 44, 46.

Since, in Gottlieb, the banked shadowed register file 30 comprises a first register 34, a second register 36, and a third register 38, Gottlieb shows no "the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer," as recited in claim 1.

Furthermore, in Gottlieb, the ability to switch between separate threads is limited by the number of the register cells 34-38 of the banked shadowed register file 30. In particular, as described at column 4, lines 47-55,

In conjunction with the register cells 20 of the standard register file 18, the register cells 34-38 of the banked shadowed register file 30 provide the ability to switch between four separate threads without accessing the memory system 22. These individual threads may be threads in the same task or threads from different tasks. In the illustrated embodiment, only one of the four threads can be active at a time, namely the thread disposed within the standard register file 18.

Since, in Gottlieb, the ability to switch between separate threads is limited by the number of the register cells 34-38, Gottlieb shows no "the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer," as recited in claim 1.

Finally, even though Gottlieb reserves the possibility of adding components to the banked shadowed register file 30 to handle additional or fewer threads or users, there will always be a predetermined number of threads which Gottlieb cannot exceed, i.e. the number of register cells. In particular, as described at column 4, lines 55-60,

Although shown supporting four separate threads, it is to be readily understood that the constituent components of the banked shadowed register file 30 can be increased or decreased to handle additional or fewer threads or users without departing from the spirit and scope of the invention.

Since, in Gottlieb, there will always be a predetermined number of threads which Gottlieb cannot exceed, Gottlieb shows no "the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer," as recited in claim 1.

Claim 1 recites further,

"said information being evacuated outside said computer."

Gottlieb neither teaches, discloses, nor suggests "said information being evacuated outside said computer," as recited in claim 1. In Gottlieb, rather, the contents of the standard register cell 20 can only be evacuated to the banked shadowed registers 34-38, as discussed above. Claim 1 is submitted to be allowable. Withdrawal of the rejection of claim 1 is earnestly solicited.

Claim 2 depends from claim 1 and adds further distinguishing elements. Claim 2 is thus also submitted to be allowable. Withdrawal of the rejection of claim 2 is also earnestly solicited.

Claims 3, 4, and 5:

Claims 3, 4, and 5 recite,

"the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer."

Gottlieb neither teaches, discloses, nor suggests "the hardware resources being used in common by a plurality of programs that are not limited in number by a total hardware resource of said computer," as discussed above with respect to the rejection of claim 1.

Claims 3, 4, and 5 recite further,

"said information being evacuated outside said computer."

Gottlieb neither teaches, discloses, nor suggests "said information being evacuated

outside said computer,” as discussed above with respect to the rejection of claim 1. Claims 3, 4, and 5 are submitted to be allowable, for at least those reasons discussed above with respect to the rejection of claim 1. Withdrawal of the rejection of claims 3, 4, and 5 is earnestly solicited.

New Claims 6, 7, and 8:

Claim 6 recites,

“a hardware resource being used in parallel by at least two of a plurality of programs.”

None of the cited references teach, disclose, or suggest “a hardware resource being used in parallel by at least two of a plurality of programs,” as recited in claim 6. Claim 6 is thus believed to be allowable.

Claim 7 recites,

“said plurality of areas being used to run at least two of a plurality of programs in parallel.”

None of the cited references teach, disclose, or suggest “said plurality of areas being used to run at least two of a plurality of programs in parallel,” as recited in claim 7. Claim 7 is thus believed to be allowable.

Claim 8 recites,

“evacuated to outside the processor.”

None of the cited references teach, disclose, or suggest “evacuated to outside the processor,” as recited in claim 8. Claim 8 is thus believed to be allowable.

Conclusion:

Accordingly, in view of the reasons given above, it is submitted that all of claims 1-8 are allowable over the cited references. Allowance of all claims 1-8 and of this entire application is therefore respectfully requested.

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If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from deposit account number 19-3935.

Respectfully submitted,

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